substantially greater than said first metal lines.

82. (Amended) The method of Claim 81 wherein said top metallization system further comprises one or more layers of metal whereby each layer of metal is separated from adjacent layers of metal by thick insulator layers of polymer, and wherein said thick insulator layers of polymer are substantially thicker than said intermetal dielectric layers.

REMARKS

Examiner Garcia is thanked for thoroughly examining the subject application. All claims are believed to be in allowable condition, and reconsideration of the rejections is respectfully requested, based on the following.

Reconsideration of the objections to Claims 3-10 and 50-55, under 37 CFR 1.75 (c), as being of improper dependent form for failing to further limit the subject matter of a previous claim, is requested, based on the following.

Claims 4-10 and 51-55 have been canceled. Claims 3 and 50 have been amended and are believed to further limit the claims on which they depend, by describing the function of the lines in the top metallization system. These claims do further limit the independent claims since they do not claim all the possible functions of top metal lines - for example, the top metal could be used as an antenna, but this is not claimed.

Reconsideration of the rejection of Claims 15, 19, 21, 81 and 82 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regard as his invention, is requested, in light of the following arguments.

Claims 15, 19, 21, 81 and 82 have been amended and are now believed to be definite.

Reconsideration of the rejection of claims 1-13, 15-28, 49-60, 62-68, and 70-83 under 35 U.S.C 103(a) as being unpatentable over Bandyopadhyay et al. in combination with Yamada '778, Yamada '020, Wolf and Cronin, is respectfully requested, based on the following arguments.

The Examiner has asserted that Bandyopadhyay, et al. "discloses formation of passivation layer 22". However, Bandyopadhyay's layer 22 is not a passivation layer, as a passivation layer is defined (and as is well known) in the semiconductor industry. Please see the attached two references (referred to as Sematech, and Wolf) that give the industry standard definition for a passivation layer. Sematech describes it as "[t]he final deposition layer in processing". See also the Wolf description, which states that "[f]ollowing patterning of the final metal layer, a passivation layer is deposited over the entire top surface of the wafers. This is an insulating, protective layer that prevents mechanical and chemical damage during assembly and packaging".

In Bandyopadhyay, et al., layer 22 is not a final layer deposited after all metal layers have been formed. It is merely a first (intermetal) dielectric, as defined at col. 5, lines 66-67. Further metal lines, such as metal lines 14 in Fig. 13, are deposited after layer 22. As seen in the Wolf description referred to above, a passivation layer is necessary to protect the underlying fine line metal, and semiconductor devices, from moisture, mobile ions and scratching. If layer 22 was a passivation layer, it would not be able to protect layer 14 from moisture and the metal lines 14 could, for example, subsequently be consumed by corrosion due to moisture. The actual passivation layer in the Bandyopadhyay structure would have to be deposited above layer 14, perhaps above other intervening fine-line metal layers.

The claimed invention describes the use of a passivation layer (layer 4 in Fig. 1) which is necessary to protect underlying fine-line metallization 3 as well as devices formed on the substrate 1. The method of the invention then continues with deposition of polymer insulating, separating layer 5, and thick, wide line metallization 10/11/12/13 (see Fig. 2), as well as polymer intermetal dielectric 14/16. This upper metal system further differentiates the claimed invention from that described in Bandyopadhyay, or the combination of Bandyopadhyay et al. with Yamada '778, Yamada '020, Wolf and Cronin, as the upper metal system does not require further passivation – the thick, wide metal is sufficiently robust that moisture protection is not required.

It is acknowledged that Bandyopadhyay is not relied on for the formation of a polymer, insulating separating layer over a passivation layer, but that Wolf instead is relied

on, at least for teaching that polyimide may be used as an intermetal dielectric (IMD). However, Wolf at pages 215-217 teaches some of the disadvantages that have caused the semiconductor industry to not use polyimide as an IMD – two examples are water absorption by the polyimide, and subsequent corrosion of underlying metal lines. Thus Wolf actually teaches away from the use of polyimide as an IMD in a fine-line metallization system. The invention, however, is not using polyimide as an IMD in the fine-line metallization system, but rather as an insulating, separating layer between the fine-line metal and the thick, wide line system above. The use of the passivation layer of the invention prevents moisture and ionic contamination from affecting the fine-line metal and devices, while the thick, wide metal system above the polymer insulating, separating layer is robust enough that moisture does not have a negative effect on reliability.

For the reasons stated above, and for the reasons given in previous responses, the claimed invention is believed to be both novel and non-obvious over the combination of Bandyopadhyay et al. with Yamada '778, Yamada '020, Wolf and Cronin. All claims are believed to be allowable, and allowance of all claims is so requested.

It is requested that should there be any problems with this Amendment, please call the undersigned Attorney at (845) 452-5863.

Respectfully submitted,

Stephen B. Ackerman, Reg. No, 37,761

Version with Markings to Show Changes Made

In the Claims

3. (Twice Amended) The method of claim 1 wherein said top metallization system contains [signal] lines [that are substantially wider than lines in said interconnecting metallization structure] that are selected from the group consisting of signal lines, power buses, ground buses or a combination thereof.

Please cancel claims 4-10.

15. (Twice Amended) The method of claim 1 wherein said insulating, separating layer of polymer [layers contains] comprises polyimide.

19. (Twice Amended) The method of claim 1 wherein said [polymer] insulating, separating [layers] layer of polymer [after said spin-on coating are] is cured at a temperature within a range of approximately 250 to 450 degrees C. for a time within a range of approximately 0.5 to 1.5 hours, said curing to occur within a vacuum or nitrogen ambient.

21. (Twice Amended) The method of claim 20 wherein [one or more of said one or more polymer insulating, separating layers after] each of said multiple processing steps of [said] spin on coating and curing [are cured] is performed at a temperature within a range of approximately 250 to 450 degrees C. for a time within a range of approximately 0.5 to 1.5 hours, said curing to occur within a vacuum or nitrogen ambient.

50. (Twice Amended) The method of claim 49 wherein said top metallization system contains [signal] lines [that are substantially wider than lines in said overlaying interconnecting metallization structure] that are selected from the group consisting of signal lines, power buses and ground buses or a combination thereof.

Please cancel claims 51-55.

81. (Amended) A method for forming a top metallization system for high performance integrated circuits comprising:

forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines in one or more layers, wherein intermetal dielectric layers are formed between said plurality of first metal lines;

depositing a passivation layer over said interconnecting metallization structure;

depositing a polymer insulating, separating layer over said passivation layer that is substantially thicker than each of [raid] said intermetal dielectric layers;

forming openings through said polymer insulating, separating layer and said

passivation layer to expose upper metal portions of said overlaying interconnecting metallization structure; depositing metal contacts in said openings; and

forming said top metallization system connected to said overlaying interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, each of said top metal lines having a width substantially greater than said first metal lines.

82. (Amended) The method of Claim 81 wherein said top metallization system further comprises one or more layers of metal whereby each layer of metal is separated from adjacent layers of metal by thick insulator layers of polymer, and wherein said thick insulator layers of [polyimide] polymer are substantially thicker than said intermetal dielectric layers.